Implementation of a Switched Capacitor Control Scheme using User-Defined Dynamic Load Models

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Abstract: The use of switched capacitor banks is very important in distribution and transmission systems for power factor and voltage regulation applications. This white paper discusses the implementation of a voltage control switch capacitor scheme by means of the user-defined dynamic modeling (UDM) tools in ETAP. The paper focuses on the controller model and its definite or inverse-time characteristic operational delays and time constants. The paper also discusses the control set points and the progressive capacitor switching implementation.

Key Words: Switched Capacitor Banks, switching capacitor controller, UDM model, power factor correction and voltage drop control

I. INTRODUCTION

The use of switching capacitors is widely used in the industry to correct power factor and under voltage conditions. Different control algorithms are available from different manufacturers, but most schemes can be generically approximated by the use of the model presented in this paper. This paper discusses the aspects of implementation of the switch-capacitor control algorithm, but does not include switching capacitor transient behavior; however, the controllers include safety factors, which prevent over-switching the capacitor banks and the potential switching transient conditions.
Switching capacitor control schemes from different manufacturers are similar. The impact of switching capacitors in this paper is viewed within the scope of steady-state voltage and power factor correction. Typical operating times of switching capacitor banks are in the range of 10 to 20 seconds to minutes and thus their inter-relation with fast voltage regulators which operate in the millisecond to seconds range is not of discussed in this paper.

A. Controller Design Objectives

The basic goals of schemes to control capacitor switching rely mainly on the following principles.

A.1 Determine the set point or controller reference parameter and apply the correct amount of capacitor banks to correct the difference between the reference and the controlled parameter.

To meet this objective the controller needs to know the deviation from the desired control value, the rate of change of the parameter, the amount of correction (kVAR to be applied) which is a factor of the magnitude of the deviation.

A.2 Minimize the range of operation and monitor over & under voltage conditions which can caused by the switching capacitor action. Determine the operational limits of the device and allow the controller to prevent damage to the system and itself.

To meet this design criterion, the controller needs to have information about the system maximum and minimum allowed voltage and current limits, the time duration of the overloads.

A.3 Control the total number of switching operations to extend the switching device operational life and minimize the frequency of switching events to prevent undesirable side effects in the system

Switching counters, which monitor the daily, weekly or monthly number of operations of the switching capacitors, are needed to limit the movement and extend the operational life of the devices.

B. Design Constraints

B.1 The size and cost of the capacitor banks

B.2 The number of switching operations allocated for the device

B.3 The amount of voltage and power factor deviation allowed along with switching transient factors will limit the design of the switching

capacitor banks and the operation and programming of its controller

II. CONTROLLER IMPLEMENTATION

The implementation of the controller to achieve the design objectives is described in three different major components:

C. PLC Controller

C.1 The implementation of the controller PLC is described in figure 1 below. The band center point indicates the middle point of the regulation dead-band. Since the operation of the switching capacitor is non-continuous, the switching action is disabled as long as the controlled parameter (which in this case is the terminal bus voltage) stays within the band defined by the lower and upper voltage limits.

Most controller manufacturers include a tolerance value on top of the upper and lower values of the band. In this design, the upper and lower value already includes the tolerance. The PLC determines how many capacitor banks need to be switched in to regulate the voltage as close as possible to the center of the dead band. Once the terminal bus voltage goes back into the band,

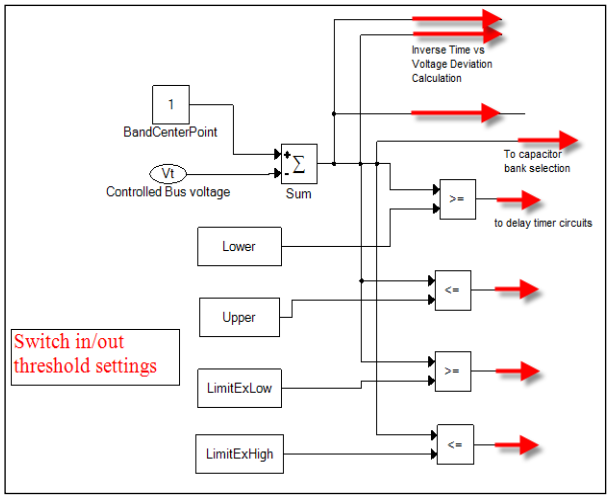


Figure 1: PLC

there is no switching action until the terminal voltage goes above or below the upper and lower value limits for a certain amount of time.

In addition, the PLC sends signals to the initial operation timers and to the extremely high or low voltage override timers. Once the initial timer reaches the pre-defined value, a second operational time delay is applied. This operation time delay can be configured in most controller models as a definite time or as an inverse-time characteristic. See figure 2.

Inverse Time Logic, (figure 3), block has been implemented based on a quadratic curve equation shown in figure 2. The higher the voltage deviation is from the desired set point, the faster the capacitor banks will switch to regulate to the desired voltage level.

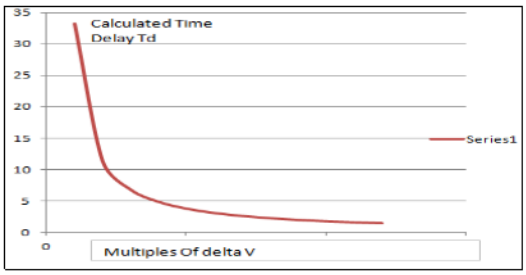


Figure 2: Inverse Time Delay Curve

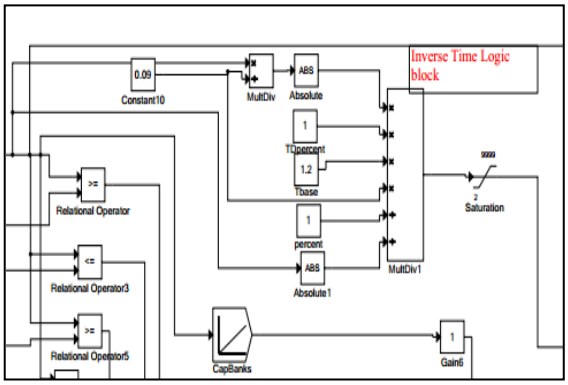


Figure 3: Inverse Time delay Logic Implementation

The timer circuit consists of a gain, automatic switch, sum, relational operator and time input (figure 4). This implementation can be used to represent a timer for any other UDM model timer. The output of the timer is channeled to the operational time delay circuit. The switching capacitor action takes place after this additional time delay has expired. Only a contactor operational time delay is added before switching in or out the capacitor banks.

The controller transfer function has five timers. The timers and their application are listed in table 1. The timers listed in table are controlled by the PLC lower, upper, LimitExLow, and LimitExHigh limits.

Table 1: Timers added to the control system

Timers Available	Purpose
Close switch	wait to add cap banks
Open switch	wait to remove cap banks
Extremely high voltage	Remove the caps
Extremely low voltage	Add the caps for severe
Operational time delay	operating time to switch in/out the cap banks

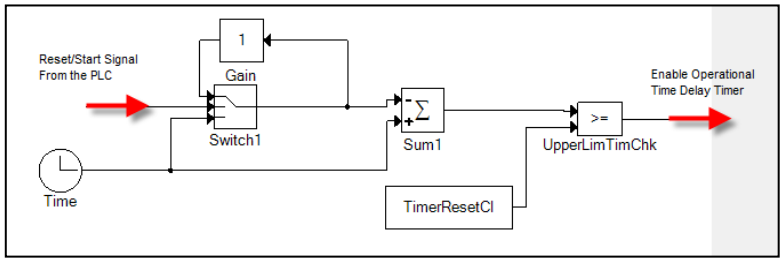


Figure 4: Timer implementation

C.2 The capacitor banks are modeled as constant impedance devices once switched on. The number of capacitor banks and the number of banks required to raise the voltage is pre-determined. For the implementation presented in this case, ten capacitor banks were used. Each bank rated at one MVAR.

The switching device time delay is modeled along with the mathematical representation of the capacitance being added to the system. Figure 5 below shows the application of constant impedance capacitor banks. The number and size of the capacitor banks are pre-determined based on the desired amount of correction.

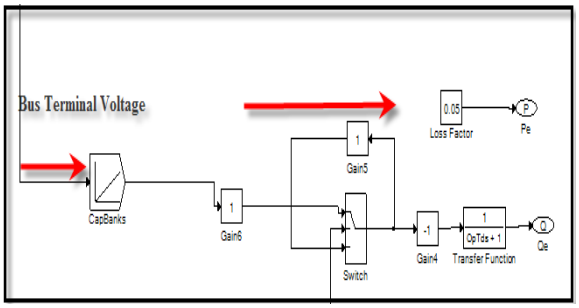


Figure 5.Definite Time Logic Implementation

The number of cap banks is selected based on the terminal bus voltage to sense the voltage. After the timer delays, the capacitor banks are switched to adjust the reactive power. The desired voltage is adjusted to improve the overall performance of the system. If the bus voltage value exceeds the extremely upper or lower thresholds, then capacitor banks are immediately switched in or out to avoid the extreme conditions system. When the bus voltage exceeds the lower or upper thresholds, the required number of capacitor banks is switched in. Please note that in other possible implementations, the capacitors may be switched in/out one at a time instead of the progressive scheme implemented here. When a definite time delay is used, the capacitor banks are switched after a fixed time delay ignoring the intensity of voltage deviation from the desired center point. When an inverse time delay is used a larger voltage deviation from midpoint will result in a smaller time delay.

III. PERFORMANCE ANALYSIS

Several transient simulation scenarios can be used to evaluate the performance of the controller. This section describes three common cases, which were used to test the controller model and transfer function.

D. *Test Scenarios*

D.1 Over and under voltage condition requiring capacitor bank operation

D.2 Severe under and over voltage conditions requiring regulator capacitor bank controller overrides

D.3 Over current conditions, which can be simulated using fault events along with overcurrent, relay elements available in the ETAP transient stability simulation package.

IV. APPLICATION EXAMPLE

This section illustrates the practical application of switched capacitor UDM model in transient stability study. In electrical systems, low voltage and high losses vary with changing operating loads. For example, industrial system loads have a higher reactive power demand, which may deteriorate the supply voltage for the rest of the network. To simulate this in ETAP, multiple scenarios were considered such as load acceptance, load rejection, and utility degraded voltage events. A simple system shown below was used to conduct the simulations.

E. *Simulations*

E.1 The switched capacitor UDM model (figure 6) is connected to the 13.8 kV main bus. As mentioned before, ten capacitor banks were used inside the model, each one rated at one MVAR. Voltage thresholds were set inside the model to determine the upper and lower limits in case of voltage variations.

Based on the following scenarios, voltage and reactive power profile for “Bus System” were observed.

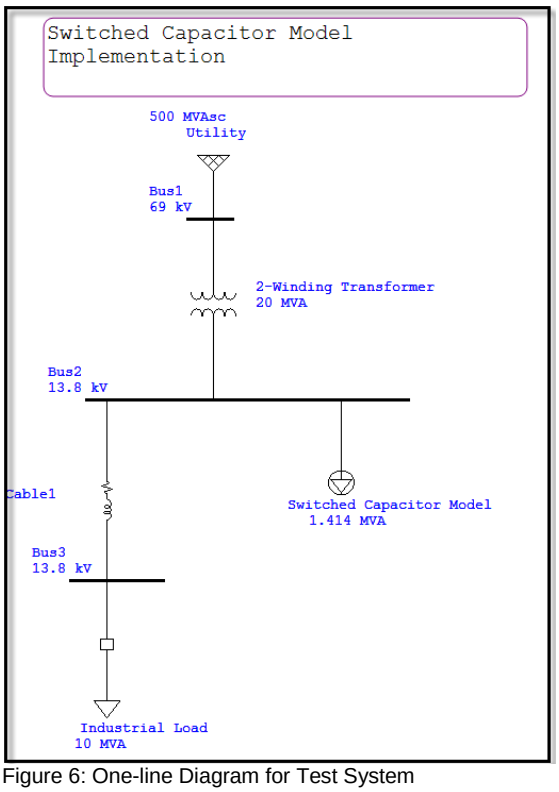


Figure 6: One-line Diagram for Test System

Table 2: Sequence of events

Sequence of Operation	Simulation Time (sec)	Bus Voltage (%)
UtilityImpact1 (-11%)	90	82
Cap Banks Switched off	115	84
Utility Impact2 (+18%)	150	98
Cap Banks Switched off completely	150.1	97.2

From table 2, it can be observed that the switched capacitor plays a very important role in maintaining a desired voltage profile. As the utility voltage drops at 90 seconds, all capacitor banks are immediately switched on because the LimitExLow limit was exceeded. As the bus voltage increased above the LimitExLow limit, the capacitor banks operate with a definite delay of 25 seconds. At 150 seconds, the utility voltage is increased above the LimitExHigh limit and all banks are immediately switched out.

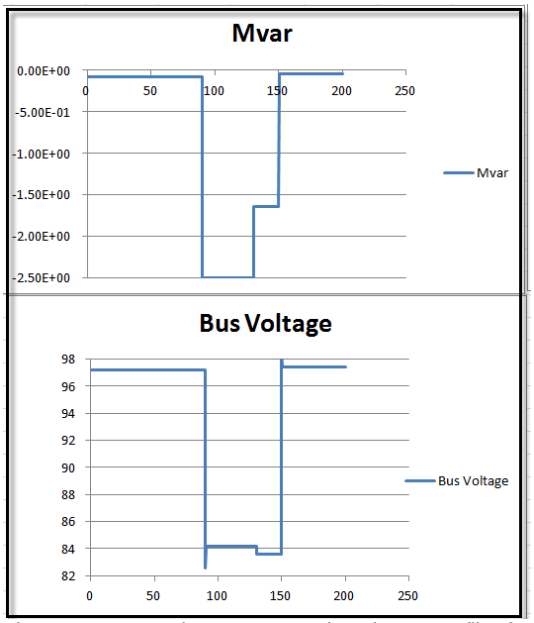


Figure 7: Reactive power and Voltage profile for definite time delay

E.2 This section describes the implementation of switching capacitor with an inverse time delay characteristic based on the same voltage deviation. This is more progressive approach to limit the losses and avoid system failure. A similar voltage profile is seen with the same utility events. The main difference is the amount of time required for the capacitor banks to operate is 15 less than the definite time. This faster time delay can be attributed to the inverse time characteristic curve. Given below are the plots of bus voltage profile when implementing the inverse time characteristic.

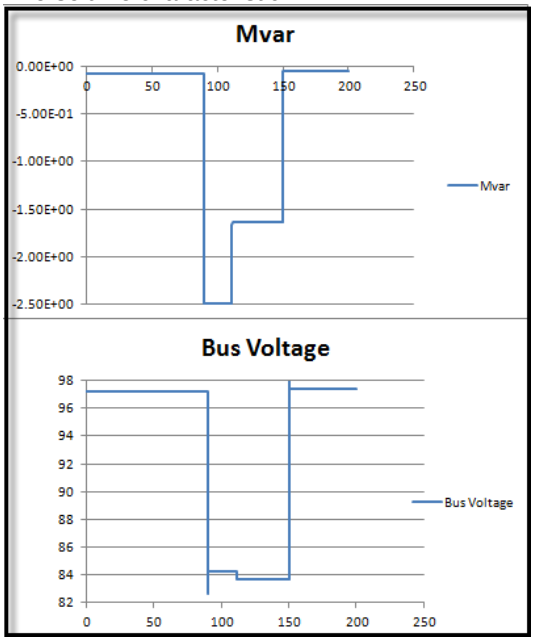


Figure 8: Reactive power and Voltage profile for inverse time delay

V. CONCLUSION

The UDM model is able to represent two different switching capacitor control mechanisms. The simpler definite time switching capacitor allows for one preset switching time. The more complex inverse time switching capacitor allows for a variable switching time depending on the amount of deviation from the set point. The UDM model is capable of representing any delay time as a function of delta V. This can be done by modifying the constants of the quadratic function of the inverse time curve. The inverse characteristic allows the switching capacitor to switch quicker to more dramatic changes in the voltage. This flexibility can lead to a more reliable system. However, a more complex control system is likely to have more components which may fail. A definite time delay control is likely to be used in systems where an event occurs consistently and causes similar disturbances. Similar disturbances allow an operator to preset a desired delay time based on their judgment. An inverse time control would be more suited for situations where disturbances are not similar and repetitive. The varying time delay allows the capacitor to accommodate different situations. These two applications are examples where distribution systems can benefit from dynamic VAR compensation. The simulations also demonstrate ETAP's capability to perform dynamic studies.

VI. REFERENCES

The following documents were consulted during the creation of this white paper:

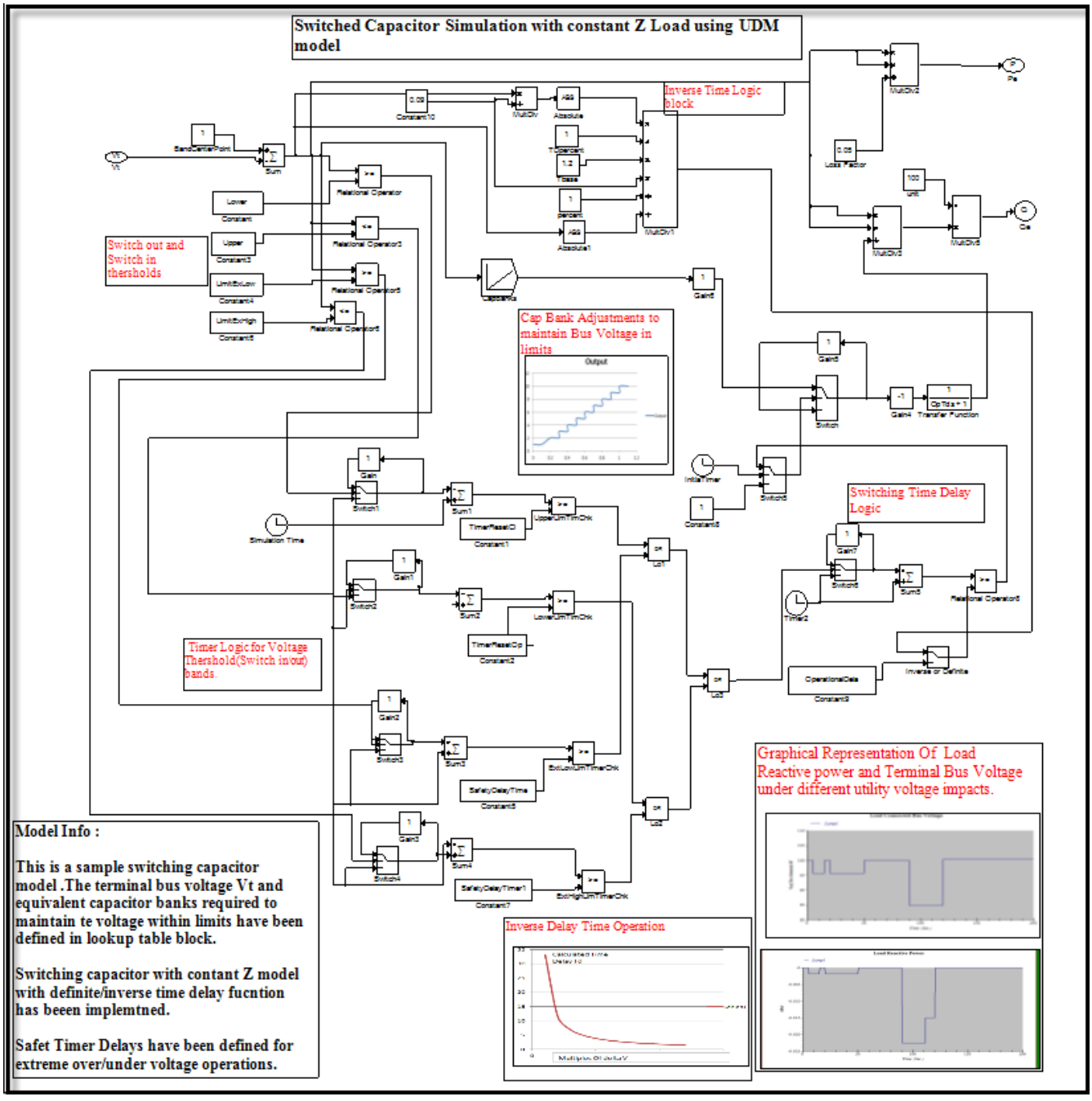
1. Kundar, Prabha. *Power system stability and control*. New York: McGraw-Hill, 1994. Print.

2. "The Multilin DGCC Capacitor Bank Controller." Multilin DGCC Controller. Version 1.10. GE Digital Energy, n.d. Web. 15 Dec. 2013. <https://www.gedigitalenergy.com/products/manuals/dgcx/dgccman-a1.pdf>

3. Greenwood, Allan. *Electrical transients in power systems.* 2. Ed. New York: Wiley, 1991. Print.

VII. APPENDIX A – TRANSFER FUNCTION

Refer to next page for UDM block diagram.


Switched Capacitor Simulation with constant Z Load using UDM model
Inverse Time Logic block
Switch out and Switch in thershold
Cap Bank Adjustments to maintain Bus Voltage in limits
Switching Time Delay Logic
Timer Logic for Voltage Thershold(Switch in/out) bands.
Graphical Representation Of Load Reactive power and Terminal Bus Voltage under different utility voltage impacts.
Inverse Delay Time Operation
Model Info :
This is a sample switching capacitor model .The terminal bus voltage Vt and equivalent capacitor banks required to maintain te voltage within limits have been defined in lookup table block.
Switching capacitor with contant Z model with definite/inverse time delay fucntion has beeen implemtned.
Safet Timer Delays have been defined for extreme over/under voltage operations.